In the Title:

Amend the title as shown below.

SPICE TO VERILOG NETLIST TRANSLATOR AND DESIGN METHODS USING SPICE TO VERILOG AND VERILOG TO SPICE TRANSLATION

In the abstract:

Please replace the abstract with the paragraph below.

Disclosed is a method for translating a SPICE format circuit description to Verilog format and design methods employing Verilog to SPICE and SPICE to Verilog translation, allowing simulation in Verilog or SPICE formats and allowing verification of Verilog to SPICE translation. SPICE to Verilog translation may employ identification of SPICE sub circuits, circuit elements, input signals, and output signals; and translation of these to Verilog format wherein signal names and design hierarchy can be maintained. Circuit element instance names may be translated to Verilog names associated with SPICE instance names. Identification and translation may employ lookup tables, rule sets, specialized field delimiters, naming conventions, or combinations thereof. An intermediate file of input and output signals may be created. SPICE node names may be converted to Verilog wire definitions.

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